ABSTRACT

An integrated circuit located between isolation trenches at the surface of a semiconductor chip comprising a first well of a first conductivity type having a first resistivity. This first well has a shallow buried region of higher resistivity than the first resistivity, extending between the isolation trenches and created by a compensating doping process. The circuit further comprises a second well of the opposite conductivity type extending to the surface between the isolation trenches, having a contact region and forming a junction with the shallow buried region of the first well, substantially parallel to the surface. Finally, the circuit has a MOS transistor located in the second well, spaced from the contact region, and having source, gate and drain regions at the surface. This space is predetermined to create a small voltage drop in I/O transistors for conditioning signals and power to a pad, or large voltage drops in ESD circuits for protecting the active circuitry connected to a pad. In the first embodiment, the space includes a dummy gate; in the second embodiment, an isolation region; in the third embodiment, the space a protected, stable surface.